UNSW GNSS Receiver development
Kevin Parkinson and Eamonn Glennon
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Namuru receiver history

We were supposed to have turned LEFT when we went warp speed out of the SNAP Lab!

We should have installed the NAMARU Board first!
UNSW receiver evolution

Namuru V1: 2004
1 RF Channel @ L1, 2MHz BW, Ethernet interface

Namuru V2: 2007
2 Channel @ L1/L2, 2MHz BW, Fast USB, RTC

Namuru V2DLR: 2011
2 RF Channels @ L1, 2MHz BW, RS422

Namuru V3: 2011
1 RF Channel @ L1, 2MHz BW
3 RF Channel @ L1/E1/L2/L5/E1 4MHz to 40MHz BW
Fast USB, RTC, Flash
Namuru V3.2 space receiver (Biarri)

- L1 2MHz BW RF FE (GP2015)
- Flash based FPGA (Actel ProASIC3)
- Flash ARM CPU (Actel SmartFusion)
- V-TCXO
- 1 MByte SRAM (EDAC)
- COLONY 2 Bus
- GPIO, RS422 & RS232
- 80mm x 80mm
V3.2 Space features

- 6 Layers
- Mechanically balanced
- RF Shielding
- SMD (Lead)
- Latch-up protection & recovery
KEA Receivers

- Small size (80mm x 55mm)
- CMOS RF ASIC’s
- FPGA Base-band
- Low power
- GPIO (Programmable)
- RTC (Battery backed)
- HS USB
- IMU (mems)
- 3 Versions (Actel, Altera & Xilinx)
- 1 or 2 RF channels
KEA V4.1S Receiver

- L1/E1 RF Channel
- CMOS RF ASIC
- SmartFusion2 MCU + FPGA
- Base-band logic
- All Flash design
- +5 or +3.3V
- Space version
KEA V4.1N Receiver

- L1/E1 RF Channel
- CMOS RF ASIC
- Altera Cyclone V FPGA
- NIOS CPU
- Base-band logic
- IO (Programmable)
- +5 or +3.3V
KEA V4.1X Receiver

- L1/E1 RF Channel
- CMOS RF ASIC
- Xilinx Artix FPGA
- Microblaze CPU
- Base-band logic
- IO (Programmable)
- +5 or +3.3V
V4Q CubeSat Interface

- Designed for KEA GNSS receivers
- CubeSat format
- PC104 Bus Interface
- PLL clock generation
- Antenna switching
KEA V4.2S Receiver

- Ch1 - L1/E1 BW 15 MHz
- Ch2 - L2 or L5/E5a BW up to 30 MHz
- Low power CMOS RF ASIC
- SmartFusion2 ARM MCU + FPGA
- Base-band logic
- All Flash design
- +5 or +3.3V
- Space version
KEA V4.2N Receiver

- Ch1 - L1/E1 BW 15 MHz
- Ch2 - L2 or L5/E5a BW up to 30 MHz
- Low power CMOS RF ASIC
- Altera Cyclone V FPGA
- Soft core NIOS CPU
- Flexible Base-band logic
- GPIO (Programmable)
- +5 or +3.3V
## Availability

<table>
<thead>
<tr>
<th>RECEIVER</th>
<th>MODEL</th>
<th>SPACE</th>
<th>L1</th>
<th>L2</th>
<th>L5</th>
<th>READY</th>
<th>FORMAT</th>
<th>BUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAMURU</td>
<td>V3.2</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td></td>
<td>NOW</td>
<td>80 x 80</td>
<td>COLONY2</td>
</tr>
<tr>
<td>KEA</td>
<td>V4.1S</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td></td>
<td>Q3 2014</td>
<td>80 x 55</td>
<td>PROG</td>
</tr>
<tr>
<td>KEA</td>
<td>V4.1N</td>
<td>Y</td>
<td>Y</td>
<td></td>
<td></td>
<td>Q3 2014</td>
<td>80 x 55</td>
<td>PROG</td>
</tr>
<tr>
<td>KEA</td>
<td>V4.1X</td>
<td>Y</td>
<td></td>
<td>Y</td>
<td></td>
<td>Q4 2014</td>
<td>80 x 55</td>
<td>PROG</td>
</tr>
<tr>
<td>KEA</td>
<td>V4.2S</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Q1 2015</td>
<td>80 x 55</td>
<td>PROG</td>
</tr>
<tr>
<td>KEA</td>
<td>V4.2N</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Q1 2015</td>
<td>80 x 55</td>
<td>PROG</td>
</tr>
<tr>
<td>KEA</td>
<td>V4.2X</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Q2 2015</td>
<td>80 x 55</td>
<td>PROG</td>
</tr>
<tr>
<td>KEA</td>
<td>V4.1SQ</td>
<td>Y</td>
<td>Y</td>
<td></td>
<td></td>
<td>Q1 2015</td>
<td>CUBESAT</td>
<td>PC104</td>
</tr>
<tr>
<td>KEA</td>
<td>V4.2SQ</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Q3 2015</td>
<td>CUBESAT</td>
<td>PC104</td>
</tr>
<tr>
<td>INTERFACE</td>
<td>V4Q</td>
<td>Y</td>
<td></td>
<td></td>
<td></td>
<td>Q4 2014</td>
<td>CUBESAT</td>
<td>PC104</td>
</tr>
</tbody>
</table>
Thank you

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